## **PRELIMINARY**

# High Performance LVDS Oscillator with Frequency Margining - Pin Control

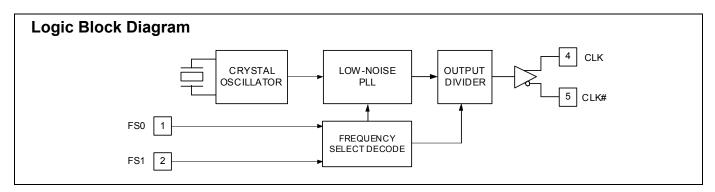
#### **Features**

- Low Jitter Crystal Oscillator (XO)
- Less than 1 ps Typical RMS Phase Jitter
- Differential LVDS Output
- Output Frequency from 50 MHz to 690 MHz
- Two Frequency Margining Control Pins (FS0, FS1)
- Factory Configured or Field Programmable
- Integrated Phase-Locked Loop (PLL)
- Supply Voltage: 3.3V or 2.5V
- Pb-Free Package: 5.0 x 3.2 mm LCC
- Commercial and Industrial Temperature Ranges

## **Functional Description**

The CY2XF33 is a high performance and high frequency Crystal Oscillator (XO). It uses a Cypress proprietary low noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed through two select pins, allowing easy frequency margin testing in applications.

The CY2XF33 is available as a factory configured device or as a field programmable device.



#### **Pinouts**

Figure 1. Pin Diagram - 6 Pin Ceramic LCC

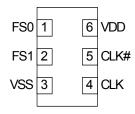


Table 1. Pin Definitions - 6 Pin Ceramic LCC

Pin	Name	I/O Type	Description
1, 2	FS0, FS1	CMOS Input	Frequency Select
4, 5	CLK, CLK#	LVDS Output	Differential Output Clock
6	VDD	Power	Supply Voltage: 2.5V or 3.3V
3	VSS	Power	Ground

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## **Functional Description**

The FS0 and FS1 pins select between four different output frequencies, as shown in Table 2. Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while the other frequencies are available for margin testing, either during product development or in system manufacturing test.

Table 2. Frequency Select

FS1	FS0	Output Frequency
0	0	Frequency 0
0	1	Frequency 1
1	0	Frequency 2
1	1	Frequency 3

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to relock.

## **Programming Description**

The CY2XF33 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described in the following sections.

#### Field Programmable CY2XF33F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyberClocks™ Online Software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using a Cypress programmer. Third party vendors manufacture programmers for small to large volume applications. Cypress's value added distribution partners also provide programming services. Field programmable devices are designated with an "F" in the part number. They are intended for quick prototyping and inventory reduction. The CY2XF33 is one time programmable (OTP).

The software is located at www.cyberclocksonline.com.

#### **Factory Configured CY2XF33**

For customers wanting ready-to-use devices, the CY2XF33 is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

### **Programming Variables**

#### **Output Frequencies**

The CY2XF33 is programmed with up to four independent output frequencies, which are then selected using the FS0 and FS1 pins. The device can synthesize frequencies to a resolution of 1 part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2XF33 has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2XF33 cannot generate frequencies in the ranges of 521 MHz to 529 MHz and 596 MHz to 617 MHz.

#### **Industrial Versus Commercial Device Performance**

Industrial and Commercial devices have different internal crystals. This has a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

#### **Phase Noise Versus Jitter Performance**

In most cases, the device configuration for optimal phase noise performance is different from the device configuration for optimal cycle to cycle or period jitter. CyberClocks Online Software includes algorithms to optimize performance for either parameter.

**Table 3. Device Programming Variables** 

Variable
Output Frequency 0 (Power on default)
Output Frequency 1
Output Frequency 2
Output Frequency 3
Optimization (phase noise or jitter)
Temperature range (Commercial or Industrial)

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## **Absolute Maximum Conditions**

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}$	Supply Voltage		-0.5	4.4	V
$V_{IN}^{[1]}$	Input Voltage, DC	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> +0.5	V
T <sub>S</sub>	Temperature, Storage	Non operating	<b>–</b> 55	135	°C
T <sub>J</sub>	Temperature, Junction		-40	135	°C
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000		V
$\Theta_{JA}^{[2]}$	Thermal Resistance, Junction to Ambient	0 m/s airflow		64	°C/W

## **Operating Conditions**

Parameter	Description	Min	Тур	Max	Unit
$V_{DD}$	3.3V Supply Voltage Range	3.135	3.3	3.465	V
	2.5V Supply Voltage Range	2.375	2.5	2.625	V
	Power Up Time for $V_{DD}$ to Reach Minimum Specified Voltage (Power Ramp is Monotonic)	0.05	-	500	ms
T <sub>A</sub>	Ambient Temperature (Commercial)	0	_	70	°C
	Ambient Temperature (Industrial)	-40	_	85	°C

## **DC Electrical Characteristics**

Parameter	Description	Condition	Min	Тур	Max	Unit
I <sub>DD</sub> <sup>[3]</sup>	Operating Supply Current	V <sub>DD</sub> = 3.465V, CLK = 150 MHz, output terminated	-	-	120	mA
		V <sub>DD</sub> = 2.625V, CLK = 150 MHz, output terminated	_	-	115	mA
V <sub>OD</sub>	LVDS Differential Output Voltage	V <sub>DD</sub> = 3.3V or 2.5V, defined in Figure 3 on page 5 as terminated in Figure 2 on page 4	250	_	450	mV
ΔV <sub>OD</sub>	Change in V <sub>OD</sub> between Complementary Output States	V <sub>DD</sub> = 3.3V or 2.5V, defined in Figure 3 on page 5 as terminated in Figure 2 on page 4	_	_	50	mV
V <sub>OS</sub>	LVDS Offset Output Voltage	V <sub>DD</sub> = 3.3V or 2.5V, defined in Figure 4 on page 5 as terminated in Figure 2 on page 4	1.125	_	1.375	V
ΔV <sub>OS</sub>	Change in V <sub>OS</sub> between Complementary Output States	$V_{DD}$ = 3.3V or 2.5V, $R_{TERM}$ = 100Ω between CLK and CLK#	_	-	50	mV
V <sub>IH</sub>	Input High Voltage		0.7*V <sub>DD</sub>	_	-	V
V <sub>IL</sub>	Input Low Voltage		_	-	0.3*V <sub>DD</sub>	V
I <sub>IH0</sub>	Input High Current, FS0 pin	Input = V <sub>DD</sub>	_	-	115	μΑ
I <sub>IH1</sub>	Input High Current, FS1 pin	Input = V <sub>DD</sub>	_	-	10	μА
I <sub>ILO</sub>	Input Low Current, FS0 pin	Input = V <sub>SS</sub>	-50	-	-	μА
I <sub>IL1</sub>	Input Low Current, FS1 pin	Input = V <sub>SS</sub>	-20	-	_	μΑ
C <sub>IN0</sub> <sup>[4]</sup>	Input Capacitance, FS0 pin		_	15	-	pF
C <sub>IN1</sub> <sup>[4]</sup>	Input Capacitance, FS1 pin		_	4	_	pF

- The voltage on any input or IO pin cannot exceed the power pin during power up.
   Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
   I<sub>DD</sub> includes ~4 mA of current that is dissipated externally in the output termination resistors.

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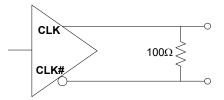


## AC Electrical Characteristics[4]

Parameter	Description	Condition	Min	Тур	Max	Unit
F <sub>OUT</sub>	Output Frequency <sup>[6]</sup>		50	-	690	MHz
FSC	Frequency Stability, commercial devices <sup>[5]</sup>	$T_A = 0$ °C to $70$ °C	-	_	±35	ppm
FSI	Frequency Stability, industrial devices <sup>[5]</sup>	$T_A = -40^{\circ} \text{ to } 85^{\circ}\text{C}$	_	_	±55	ppm
AG	Aging, 10 years		_	-	±15	ppm
T <sub>DC</sub>	Output Duty Cycle	F <= 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T <sub>R</sub> , T <sub>F</sub>	Output Rise and Fall Time	20% and 80% of full output swing	_	350	1	ps
T <sub>LOCK</sub>	Startup Time	Time for CLK to reach valid frequency measured from the time V <sub>DD</sub> = V <sub>DD</sub> (min)	_	_	10	ms
T <sub>LFS</sub>	Re-lock Time	Time for CLK to reach valid frequency from FS0 or FS1 pin change	_	_	10	ms
T <sub>Jitter(\phi)</sub>	RMS Phase Jitter (Random)	f <sub>OUT</sub> = 106.25 MHz (12 kHz–20 MHz)	_	1	_	ps

## **Termination Circuits**

Figure 2. LVDS Termination



#### Notes

- Not 100% tested, guaranteed by design and characterization.
   Frequency stability is the maximum variation in frequency from F<sub>0</sub>. It includes initial accuracy, plus variation from temperature and supply voltage.
   This parameter is specified in CyberClocks Online software.



## **Switching Waveforms**

Figure 3. Output Voltage Swing

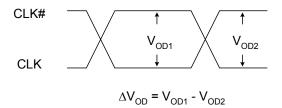


Figure 4. Output Offset Voltage

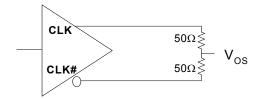


Figure 5. Output Duty Cycle Timing

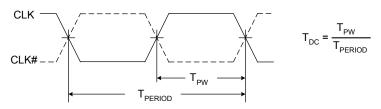


Figure 6. Output Rise and Fall Time

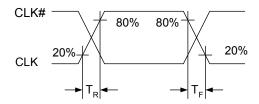
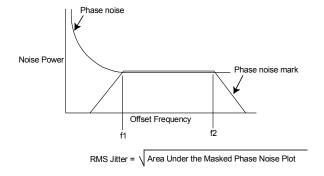


Figure 7. RMS Phase Jitter



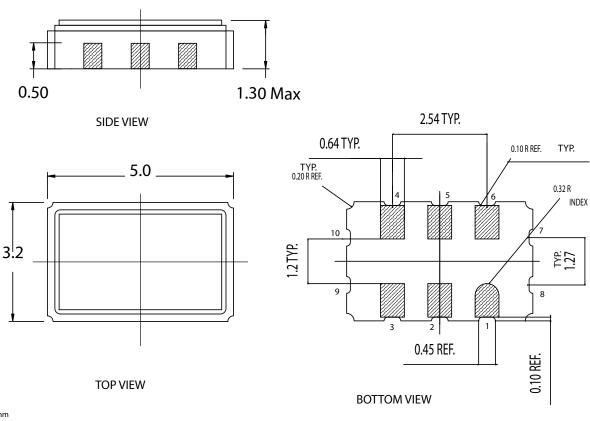


## **Ordering Information**

Part Number <sup>[7]</sup> Configuration		Package Description	Product Flow	
Pb-Free				
CY2XF33FLXCT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C	
CY2XF33FLXIT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C	
CY2XF33LXCxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C	
CY2XF33LXIxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C	

## **Package Drawings and Dimensions**

Figure 8. 6-Pin 3.2x5.0 mm Ceramic LCC LZ06A



Dimensions in mm General Tolerance: ± 0.15MM Kyocera dwg ref KD-VA6432-A Package Weight ~ 0.12 grams

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Note
7. "xxx" is a factory assigned code that identifies the programming option.



## **Document History Page**

Document Title: CY2XF33 High Performance LVDS Oscillator with Frequency Margining - Pin Control Document Number: 001-53148						
REV.	REV. ECN NO. Orig. of Change Date Description of Change					
**	2704379	KVM/PYRS	05/11/2009	New data sheet		
*A	2734005	WWZ	07/09/2009	Post to external web		

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